In the Specification:

Please replace the paragraph beginning on page 7, line 22 with the following rewritten paragraph:

On both sides of a channel layer 3' of the current path pattern 3 in the cross area 10, the LDD structure is formed which has a low concentration region in contact with the channel layer and a high concentration region in contact with the low concentration region. In areas in contact with the channel layer 3" in the cross area 11, a low concentration region is not formed. Namely, the high concentration regions are in direct contact with this channel layer. This high concentration region has an impurity concentration higher than that of the low concentration region in the cross area 10.

Please replace the paragraph beginning on page 9, line 25 with the following rewritten paragraph:

Next, by using the gate bus line 1 and gate insulating film 22a as a mask, a second phosphorous ion doping is performed. The second phosphorous ion doping is performed under the conditions of an acceleration energy of 10 keV and a dose of 5×10^{15} cm^{-2}. In the cross area 11, high concentration regions 3e are therefore formed on both sides of the channel layer 3" just under the gate bus line 1. In the cross area 10, a high concentration region 3e in contact with the low concentration region 3d is therefore formed.

Please replace the paragraph beginning on page 11, line 4 with the following rewritten paragraph:

As shown in Fig. 2D, the current path pattern 3 has, on both sides of the channel layer in the cross area 10, the low concentration regions 3d in contact with the channel layer and the high concentration regions 3e in contact with the low concentration regions 3d, constituting the LDD structure. The channel layer 3" in the cross area 11 is in direct contact with the high concentration regions 3e having an impurity concentration higher than that of the low concentration region 3d.

Please replace the paragraph beginning on page 15, line 17 with the following rewritten paragraph:

A p-channel type TFT 41 in the peripheral circuit area 36 is constituted of a current path pattern 41C, an end portion 41S on the source side, an end portion 41D on the drain side, and a gate electrode 41G. The current path pattern 41C includes a portion in which current flows in the ~~column~~ row direction. The gate electrode 41G extends in the row direction and crosses the column directionally flowing current portion of the current path pattern 41C.

Please replace the paragraph beginning on page 16, line 15 with the following rewritten paragraph:

TFT 40 in the image display area 35 has the double-gate structure and the LDD structure on the source side of the gate near the source and on the drain side of the gate near the drain. Therefore, as compared to a TFT ~~without~~ with no LDD structure, the off-current can be reduced more. In the peripheral circuit area, desired TFTs are provided with the one-side LDD structure, and other TFTs are not provided with the LDD structure. For example, n-channel type TFTs are provided with the one-side LDD structure and p-channel type TFTs are not provided with the LDD structure. In this manner, the reliability of n-channel type TFTs can be improved and the on-current of p-channel type TFTs can be prevented from being lowered.

Please replace the paragraph beginning on page 17, line 21 with the following rewritten paragraph:

Fig. 8C shows a TFT having a narrow gap between two branched gate electrodes. A low concentration region LDD formed on one side in one cross area reaches the border of the gate electrode G in the other cross area. The LDD structure is formed on both sides of the gate electrode in one cross area. By properly setting the incidence angle of ~~a~~ an irradiated laser beam and the gap between the branched gate electrodes, the LDD structure can be formed on both ~~side~~ sides in one cross area. The LDD structures on both

sides of a channel layer can suppress a variation in element characteristics when the polarity of voltage applied to TFT is inverted.